What is claimed is:

1. A circuit, comprising:

a first switching element coupled to a first terminal and a second terminal;

a second switching element coupled to the first terminal; and

a capacitor coupled between the second switching element and a ground or reference voltage.

2. The circuit of claim 1, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second switching element between high and low.

3. The circuit of claim 2, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

4. The circuit of claim 1, wherein

the first terminal is a high impedance node,

the second terminal is a low impedance node, and

the circuit operates to substantially null and cancel the charge injection and clock feed-through error voltage, respectively, by absorbing the charge injection into the capacitor and by generating a compensation signal.

5. The circuit of claim 4, wherein the circuit replaces a switching element in a switched network.

6. A switching element, comprising:

a circuit including a first switching element coupled to a first terminal and a second terminal, a second switching element coupled to the first terminal, and a capacitor coupled between the second switching element and a ground or reference voltage.

7. The switching element of claim 6, wherein the circuit substantially nulls a charge injection by absorbing the charge injection into the capacitor and canceling the feed-through error voltage by generating a compensation signal with opposite polarity at the first terminal.

8. The switching element of claim 7, wherein the circuit replaces another switching element in the switched network.

9. The switching element of claim 8, wherein the another switching element is at a location in the switched network where a charge injection or a clock feed-through error voltage is high.

10. A method of nulling a charge injection and a clock feed-through error voltage in a switched network, comprising:

replacing at least one switching element in the switched network with a nulling circuit, the nulling circuit nulling the charge injection by absorbing the charge injection in a capacitor.

11. The method of claim 10, further comprising:

generating a compensation signal such that the clock feed-through error voltage has been removed.

12. A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, injecting a clock feed-through error voltage and a charge injection into a first terminal; and

switching a second switching element to on by turning a second clock signal to high, nulling the clock feed-through error voltage and charge injection as a result of the opposite signal polarities and absorbing the charge injection into a capacitor, respectively.

13. A method of nulling a charge injection in a switched network, comprising: injecting a terminal with a stored channel charge and clock feed-through voltage; and nulling the charge and voltage injected into the terminal by absorbing the charge in a capacitor and canceling the voltage by a compensation signal with opposite polarity.

14. The method of claim 13, wherein

the injecting occurs as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch such that the second switch is turned on, resulting in the compensation signal.

15. A circuit, comprising:

a first switching element coupled to a first node and a second node;

a second switching element coupled to the first node;

a third switching element coupled to the second node;

a first capacitor coupled between the second switching element and a ground or reference voltage; and

a second capacitor coupled between the third switching element and the ground or reference voltage.

16. The circuit of claim 15, further comprising:

a first clock signal to switch the first switching element between high and low; and

a second clock signal to switch the second and third switching elements between high and low.

17. The circuit of claim 16, wherein the second clock signal is the phase-shifted complementary signal of the first clock signal.

18. The circuit of claim 15, wherein

the first node is a high impedance node,

the second node is a high impedance node,

the circuit operates to substantially null and cancel the charge injection and clock feed-through error voltage, respectively, by absorbing the charge injection into the first and second capacitors and by generating a compensation signal on the first and second nodes.

19. The circuit of claim 18, wherein the circuit replaces a switching element in a switched network.

20. A switching element, comprising:

a circuit including a first switching element coupled to a first node and a second node, a second switching element coupled to the first node, a third switching element coupled to the second node, and a first capacitor coupled between the second switching element and a ground or reference voltage, and a second capacitor coupled between the third switching element and a ground or reference voltage.

21. The switching element of claim 20, wherein the circuit substantially nulls a charge injection by absorbing the charge injection into the first and second capacitors and canceling the feed-through error voltage by generating a compensation signal with opposite polarity at the first and second nodes.

22. The switching element of claim 21, wherein the circuit replaces another switching element in a switched network.

23. The switching element of claim 22, wherein the another switching element is at a location in the switched network where a charge injection or a clock feed-through error voltage is high.

24. A method of nulling a charge injection and a clock feed-through error voltage in a switched network, comprising:

replacing at least one switching element in the switched network with a nulling circuit, the nulling circuit nulling the charge injection by absorbing the charge injection in a first capacitor and a second capacitor.

25. The method of claim 24, further comprising:

generating a compensation signal on a first node and a second node such that the clock feed-through error voltage has been removed.

26. A method of nulling a charge, comprising:

switching a first switching element to off by turning a first clock signal to low, injecting a clock feed-through error voltage and a charge injection into a first node and a second node; and

switching a second switching element and a third switching element to on by turning a second clock signal to high, nulling the clock feed-through error voltage and charge injection as a result of the opposite signal polarities and absorbing the charge injection into a first capacitor and a second capacitor.

27. A method of nulling a charge injection in a switched network, comprising:

injecting a first node and a second node with a stored channel charge and clock feed-through voltage; and

nulling the charge and voltage injected into the first and second nodes by absorbing the charge in a first capacitor and a second capacitor and canceling the voltage by a compensation signal with opposite polarity on the first and second nodes.

28. The method of claim 27, wherein

the injecting occurs as a result of providing a first clock signal to a first switch such that the first switch is turned off, and

the nulling occurs as a result of providing a second clock signal to a second switch and a third switch such that the second and third switches are turned on, resulting in the compensation signal on the first and second nodes.